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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/197,993	11/23/1998	STEVEN EUGENE LOVETTE		1952

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EXAMINER

NGUYEN, DUSTIN

ART UNIT PAPER NUMBER

2154

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/197,993	Applicant(s) LOVETTE, STEVEN EUGENE	
	Examiner Dustin Nguyen	Art Unit 2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 26-49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 26-49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 26 – 49 are presented for examination.

Response to Arguments

2. Applicant's arguments filed 02/02/2006 have been fully considered but they are not persuasive.
3. As per remarks, Applicants' argued that (1) that the Cowan reference teaches storing a predetermined value in a location adjacent to a return address within the stack, rather than storing a predetermined value in a first address location immediately preceding the starting location of the stack, as recited in claim 26.
4. As to point (1), the Meriam-Webster's Collegiate Dictionary defines stack as a memory or a section of memory in a computer for temporary storage in which the last item stored is the first item retrieved. In this case, Figure 2 of Cowan shows a "canary word" storing location [i.e. a predetermined value in a first address location] is before or ahead [counting from the bottom up since item is inserted at the top of the stack] [i.e. immediately preceding] of a "return address" storing location [i.e. the starting location of the stack] [Figure 2; and paragraphs 1 and 2, page 7].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 26-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta [US Patent No 5,222,220], in view of Cowan et al. "StackGuard: Automatic Adaptive Detection and Prevention of Buffer-Overflow Attacks".

7. As per claim 26, Mehta discloses the invention substantially as claimed including a method for detecting corruption associated with a stack in storage device, the method comprising the steps of:

detecting the occurrence of a stack operation within the stack [i.e. detecting subroutine or interrupt logic [jump, branch]] [col 3, lines 12-21 and lines 49-54]; and

comparing the value in the first address location to the first predetermined value to determine if the stack operation corrupted the first predetermined value stored in the first address location [i.e. the return address is compared with the address in the return address latch register] [48, Figure 3; Abstract; col 3, lines 59-col 4, lines 17; and col 5, lines 38-col 6, lines 10].

Mehta does not specifically disclose

storing a first predetermined value in a first address location immediately preceding the starting location of the stack.

Cowan discloses

storing a first predetermined value in a first address location immediately preceding the starting location of the stack [Figure 2; paragraphs 1 and 2, page 7].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Mehta and Cowan because Cowan's teaching of storing a value preceding the starting location of the stack would allow to prevent the buffer overflow attacks [Cowan, paragraph 5, page 3].

8. As per claim 27, Mehta discloses the first determined value comprises a known bit pattern [i.e. store address in a latch register] [40, Figure 3; and col 3, lines 41-45].

9. As per claim 28, Mehta discloses wherein the first predetermined value comprises a processor readable address [i.e. return address] [Abstract; and col 3, lines 41-45].

10. As per claim 29, Mehta does not disclose wherein the first predetermined value comprises a processor readable instruction. Cowan discloses wherein the first predetermined value comprises a processor readable instruction [i.e. one per function in the object code] [paragraph 8, page 9]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Mehta and Cowan because Cowan's teaching would allow introduce another level of security to the system.

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11. As per claims 30 and 31, Cowan discloses wherein the stack operation inserts data in the stack and removes data from the stack [i.e. push, pop] [page 11].

12. As per claim 32, Mehta discloses the step of storing a second predetermined value in a second address location immediately following the ending location of the stack [i.e. write stack boundary to high and low registers] [Figure 5; and col 4, lines 24-46].

13. As per claims 33-35, they are rejected for similar reasons as stated above in claims 27-29.

14. As per claims 36 and 37, they are rejected for similar reasons as stated above in claims 30 and 31.

15. As per claims 38-49, they are apparatus claimed of claims 26-37, they are rejected for similar reasons as stated above in claims 26-37.

16. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (571) 272-3971. The examiner can normally be reached on flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Follansbee John can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
Dustin Nguyen
Examiner
Art Unit 2154